

Serial No. 10/620,119
Attorney Docket No. 015559-288
Amendment

IN THE DRAWINGS:

Replace original Figs. 1-19 with attached replacement Figs. 1-19.

Remarks

The drawings and claims 28, 31-33, 36, 46, 47, and 50-55 have been amended. Claims 1-27, 29, 30, 57-68, 72, 74, 80-86, 88, 89, 91-94, 96 and 98 have been cancelled and new claims 113-122 have been added. Review and reconsideration in light of the amendments and remarks below are respectfully requested.

The drawings have been amended to provide formal drawings and replace the originally-filed informal drawings. Thus it is submitted that the objection to the drawings has been properly addressed.

Claims 28, 29, 33, 37, 39-41, 43-48, 50, 51 and 53-55 are rejected as being anticipated by U.S. Pat. No. 6,587,613 to De Natale. In addition, claims 30-32, 34-36, 38, 42, 49, 52 and 56 are rejected as defining obvious subject matter over De Natale.

Accordingly, claim 28 has been amended to include the subject matter of claims 29 and 30, and claims 29 and 30 have been canceled. To the extent that the rejection of claim 30 would be carried over to amended claim 28, such rejection is respectfully traversed.

As amended claim 28 now specifies that the upper wafer defines a coverage area in top view. Claim 28 also now specifies that the solderable surface is not located within the coverage area. In the rejection of claim 30 (at page 5), the Office action indicates that it would have been obvious at the time the invention was made that either the upper or lower portion of the De Natale reference would have a top view. Applicants do not dispute this position as any component can have a top view. However, the Office action then goes on to state "*Therefore, the upper wafer portion would define a coverage area in the top view and the solderable surface is not located within the coverage area...*" (emphasis added). However, Applicants respectfully traverse this statement.

It is noted that simply because an upper wafer portion may define a coverage area in top view, it does not necessarily follow that the solderable surface is not located in the coverage area. In fact, the De Natale reference the exact opposite relation is true. It appears that the Office action has construed the contacts 82 of the De Natale reference (see Fig. 6) as the claimed

solderable surface. However, the contacts 82 of the De Natale reference are squarely within the coverage area of the upper wafer portions 50, 60, 70. In fact, as can be seen in Fig. 6 each of the contacts 82 are located directly below the upper wafer portions 50, 60, 70 and are therefore located in the coverage area. It is noted that Fig. 6 of De Natale illustrates a cross section of that device and a top view would be, for example, a top view of the device shown in Fig. 10.

In contrast, claim 28, as amended, specifies that the solderable surface is not located within the coverage area of the upper wafer. For example, as shown in Fig. 7 of this application, the solder pads 80 are not located within the coverage area of the upper wafer 34. In Fig. 7 the solder pads 80 are not located below the upper wafer 34 and are laterally offset therefrom.

As noted at page 10, 2nd full paragraph of this application, locating each of the connection sites 88/solder pads 80 outside of the coverage area of the upper wafer allows each of the connection sites 88 to be easily accessed. For example, as shown in Fig. 8 of this application, a chip 81 can be easily coupled to the connection site 88 from a front side of the mirror array. In contrast, in the De Natale reference, the only way in which the contacts 82 of Fig. 6 can be accessed is from the underside of the mirror array.

In addition, locating the solderable surface not within the coverage area of the upper wafer may be the result of certain advantageous manufacturing processes. During an early part of the manufacturing process the connection sites 88 are located below, and protected by, the upper wafer 34, as shown in Fig. 9. The configuration provides protection to the connection sites 88 during certain processing steps. In particular, aggressive etching steps, which may be harmful to the connection sites 88, may be carried out while the assembly is in its configuration of Fig. 9 which leaves the connection sites protected.

When it is desired to singulate the individual mirror arrays, the assembly of Fig. 9 is cut or singulated along an offset line 97 (see Fig. 10). The offset nature of this cut 97 exposes the connection site 88 such that it is not within the coverage area of the upper wafer 34, and is easily accessible for connection.

Thus, in sum, it is submitted that the De Natale reference does not disclose, teach or suggest a solderable surface that is not within the coverage area of the upper wafer. The Office action also does not cite to any secondary reference which discloses this claim limitation, provide a motivation to combine the references, etc. in the manner required for a proper *prima facie* case of obviousness under MPEP §2143. Thus it is submitted that claim 28, as amended, is not obvious over the De Natale reference.

Independent claim 56 is somewhat analogous to claim 28 in that claim 56 specifies that the electronic component is generally not located within the coverage area of the upper wafer portion. In contrast, what the Office action has construed as the claimed electrical component (drive electrode 66) is squarely within the coverage area of the upper wafer portion of the De Natale reference (see Fig. 7). This is submitted that claim 56 is allowable over the De Natale reference.

New independent claim 118 similarly specifies that the solderable surface is not located inside the coverage area of the upper wafer portion, which is not shown in the De Natale reference. In addition, claim 118 also specifies that the lower wafer portion includes at least one electrode for controlling the movement of at least part of the microstructure. The Office action has construed electrode 66 of the De Natale reference as the claimed electrode. However, claim 118 also claims an electronic component coupled to the solderable surface by flip chip bonding, wherein the electronic component is electrically or operatively coupled to the electrode. The Office action appears to construe the electrode 66 of the De Natale reference as the claimed electronic component (in addition to the claimed electrode). Thus it is submitted that the De Natale reference further fails to disclose at least one of the electrode/electronic component of claim 118.

Without acceding to the propriety of the rejection of any claim not specifically addressed herein, the rejection of selected dependent claims are briefly discussed below. Claim 34 specifies that the upper and lower wafers are coupled together by a photopatternable adhesive. The Office action indicates that the De Natale reference does not limit the coupling of the two

Serial No.: 10/620,119
Attorney Docket No.: 015559-288
Amendment

wafers to soldering or flip chip bonding techniques. However, the De Natale reference does not disclose the subject matter of claim 34, nor does the Office action cite to any secondary reference as including the subject matter of claim 34.

The Office action takes the position that adhesives are widely used to bond wafers. However, the wafers of the De Natale reference are already coupled together by soldering or flip chip bonding in order to make the proper electrical connections. Thus there would be no need to utilize an adhesive in addition to the soldering or flip chip bonding. Accordingly the rejection of claim 34 is respectfully traversed.

Should the Office continue to reject claim 34, it is requested that the Office produce some reference which teaches the claimed subject matter and proposes why and how the references would be combined to show the subject matter of claim 34 in the manner required for a proper *prima facie* case of obviousness under MPEP §2143. The remarks made above with respect to claim 34 apply equally to claims 35 and 36.

Claim 39 depends from claim 28 and specifies that the system further includes an electronic component coupled to the solderable surface such that the electronic component can control, provide inputs to or receive outputs from the microstructure. The Office action (at page 3) indicates that the drive electrode 66 of De Natale is considered to correspond to the claimed electronic component. Claim 40 depends from claim 39 and specifies that the electronic component is a chip that is coupled to the solderable surface by flip chip bonding. However, the drive electrode 66 of the De Natale reference is not a chip and is not coupled to the solderable surface by flip chip bonding. Accordingly the rejection of claim 40 is respectfully traversed, and further explanation is required should the rejection be maintained.

Claim 47 claims at least two electrodes located below each reflective surface. The Office action takes the position that De Natale discloses at least two electrodes 66 below each reflective surface. However, it appears that De Natale discloses only a single electrode 6 (see Fig. 7) below each reflective surface. Accordingly the rejection of claim 47 is respectfully traversed and further explanation is requested.

Serial No.: 10/620,119
Attorney Docket No.: 015559-288
Amendment

New claim 113 depends from claim 28 and specifies that the upper wafer portion and lower wafer portion are coupled together by an electrically insulating material such that the upper and lower wafer portions are not directly electrically connected. For example, at page 7 lines 5-6 of this application it is indicated that the bond between the upper and lower wafers can be electrically insulating. In contrast, the upper and lower wafers of De Natale are electrically coupled. New claim 119 depends from claim 118 and includes similar limitations.

New claims 114-117, 120 and 121 further distinguish over the De Natale reference.

New claim 122 specifies that the electronic component is positioned generally between the upper and lower wafer portions. In contrast, the De Natale reference does not disclose this claim limitation.

Claim 51 has been amended to clarify that the reflective surfaces are non-silicon. In contrast in the De Natale reference the upper silicon surfaces function as the reflective surfaces.

Claims 31-33, 36, 46, 47, 50 and 52-55 have been amended to accommodate the amendment of claim 28, and/or to improve the clarity of those claims.

Thus, in sum, it is submitted that the application is in a condition for allowance, and formal notice thereof is respectively solicited.

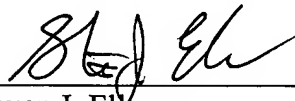
The Office action (at page 7) indicates that the documents submitted in Applicants' Information Disclosure Statement have been considered and made of record. However, it is noted that two documents were not initialed by the Examiner. These documents are: 1) U.S. Publication No. 2003/0107794 to Siekkinen et al. and 2) the article entitled "Low Temperature Wafer-Level Transfer Bonding" by F. Niklaus et al. and published in the Journal of Microelectrical Systems. These references are listed at the top-most portion of the pages of Applicants' Information Disclosure Statement, and thus the lack of initials appears to be a mere oversight. However Applicants request that the Examiner initial these two references and send Applicants a copy of the fully initialed list of references. The Examiner is invited to contact the undersigned should additional copies of these references be required.

A Petition for Correction of Inventorship accompanies this Amendment.

Serial No.: 10/620,119
Attorney Docket No.: 015559-288
Amendment

The Commissioner is hereby authorized to charge any additional fees required, including the fee for an extension of time; or to credit any overpayment to Deposit Account 20-0809. The applicant(s) hereby authorizes the Commissioner under 37 C.F.R. §1.136(a)(3) to treat any paper that is filed in this application which requires an extension of time as incorporating a request for such an extension.

Respectfully submitted,



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